What is claimed is:

1. A method for enhancing the security of a system operating in conjunction with a clock signal from a system clock, comprising:

monitoring the system for detecting a fault in the system;

upon detection of a fault, switching the system from operating in conjunction with a clock signal from the system clock to operate in conjunction with a secure clock signal from a secure clock.

2. The method of claim 1, wherein the system is switched to operate in conjunction with a secure clock signal from one of a plurality of secure clocks.

3. The method of claim 1, further comprising:

monitoring the system operating in conjunction with a clock signal from a secure clock,

upon detecting cessation of said fault in the system, switching the system to again operate in conjunction with a clock signal from the system clock.

4. The method of claim 3, further comprising switching the system back to the clock signal from the system clock even if the system clock is not operating.

5. The method of claim 1 further comprising monitoring the system for detecting a fault associated with one of an over-frequency and under-frequency clock signals from the system clock.

6. The method of claim 1, further comprising:

when switching the system to operate in conjunction with the secure clock signal from the secure clock, preventing the clock signal from having short transitions that do not cross the logic threshold from a high to low state or a low to high state.

7. The method of claim 1, wherein when switching from the clock signal of the system clock to the secure clock signal of the secure clock, the clock signal has an extend low time.

8. The method of claim 1 further comprising multiplexing together clock signals from the system clock and from at least one secure clock and, upon detecting a fault, selecting one of the multiplexed clock signals for operating the system.

9. The method of claim 3 further comprising, when switching between clock signals, waiting until the clock signal, which is being switched from, transitions to a low state.

10. An apparatus for enhancing the security of a system operating in conjunction with a clock signal from a system clock, the apparatus comprising:

a secure clock generating a secure clock signal;

a clock monitor circuit configured to monitor the system for detecting a fault;

clock switching circuitry, the clock switching circuitry operably coupled to the clock monitor circuit, the system clock signal and the secure clock signal;

the clock switching circuitry configured, upon the detection of a fault, to switch the system from operating in conjunction with a clock signal from the system clock to operate in conjunction with a secure clock signal from a secure clock.

11. The apparatus of claim 10, further comprising:

a plurality of secure clocks with secure clock signals;

the clock switching circuitry operably coupled to plurality of secure clock signals for switching the system to operate in conjunction with one of the secure clock signals.

12. The apparatus of claim 10, wherein the secure clock includes a ring oscillator.

13. The apparatus of claim 10, wherein the clock monitor circuit is configured to detect the cessation of the detected fault;

the clock switching circuitry further configured to switch the system to again operate in conjunction with a clock signal from the system clock upon detecting the cessation of said fault.

14. The apparatus of claim 10 wherein the clock monitor circuit is configured to monitor the system for detecting a fault associated with one of an over-frequency and under-frequency clock signals from the system clock, the clock switching circuitry configured to switch the system to operate in conjunction with a secure clock signal from a secure clock to prevent over-frequency and under-frequency clocking of the system.

15. The apparatus of claim 14 wherein the clock monitor circuit includes frequency dividers; and, delay lines, the frequency dividers and delay lines configured to detect over-frequency and under-frequency clock signals from the system clock.

16. An application specific integrated circuit comprising:

a processor;

a clock generating a system clock signal for operation of the processor;

the secure clock further generating a secure clock signal;

a clock monitor circuit configured to monitor the application specific integrated circuit

for detecting a fault;

clock switching circuitry, the clock switching circuitry operably coupled to the clock monitor circuit, the system clock signal and the secure clock signal;

the clock switching circuitry configured, upon the detection of a fault, to switch the processor from operating in conjunction with a system clock signal to operating in conjunction with the secure clock signal.

17. The circuit of claim 16, further comprising:

a plurality of secure clocks with secure clock signals;

the clock switching circuitry operably coupled to plurality of secure clock signals for switching the system to operate in conjunction with one of the secure clock signals.

18. The circuit of claim 16, wherein the clock monitor circuit is configured to detect the cessation of the detected fault;

the clock switching circuitry further configured to switch the processor to again operate in conjunction with the system clock signal upon detecting the cessation of said fault.

19. The circuit of claim 16 wherein the clock monitor circuit is configured to monitor the circuit for detecting a fault associated with one of an over-frequency and under-frequency system clock signal, the clock switching circuitry configured to switch the processor to operate in conjunction with a secure clock signal from a secure clock to prevent over-frequency and under-frequency clocking of the processor.